O.P.Code: 23EC0421	R23	H.T.No.									

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech. III Year II Semester Regular Examinations April-2026

VLSI DESIGN

(Electronics & Communications Engineering)

Time: 3 Hours **Max. Marks: 70**

PART-A

(Answer all the Questions **10 x 2 = 20** Marks)

1	a	Define MOS technology.	CO1	L1	2M
	b	Define figure of merit (ω0) in MOS devices.	CO1	L1	2M
	c	What is meant by VLSI Design Flow?	CO3	L1	2M
	d	State two limitations of MOS scaling.	CO3	L1	2M
	e	Define Switch Logic in VLSI design.	CO4	L1	2M
	f	What does fan-in and fan-out mean in digital circuits?	CO5	L1	2M
	g	What are the main parameters influencing low power design in VLSI?	CO4	L2	2M
	h	Differentiate between FPGA and CPLD architectures based on logic structure and configuration.	CO5	L4	2M
	i	Define scan chain in scan design technique.	CO6	L1	2M
	j	What is the difference between testing combinational and sequential circuits?	CO6	L2	2M

PART-B

(Answer all Five Units **5 x 10 = 50** Marks)

UNIT-I

2		Determine the relationship between Ids & Vds in non-saturated region.	CO2	L3	10M

OR

3	a	Show the circuit diagram of BiCMOS inverter and explain its operation	CO2	L2	5M
	b	Derive the expression for threshold voltage for MOS transistors	CO2	L2	5M

UNIT-II

4	a	Explain the basic NMOS inverter circuit with neat diagram and its operation.	CO3	L2	5M
	b	Construct layout diagram for the logic equations in CMOS logic. $Z = (AB + CD)E$	CO3	L3	5M

OR

5	a	Sketch the layout diagram for CMOS inverter.	CO3	L3	5M
	b	Explain about Implant and demarcation line in stick diagrams with neat sketches.	CO3	L2	5M

UNIT-III

6	a	What is pseudo NMOS logic? Explain with an example	CO4	L1	5M
	b	Explain the problem of driving large capacitive loads.	CO5	L2	5M

OR

7	a	Construct 2-input NAND gate by using pseudo NMOS logic.	CO4	L3	5M
	b	Discuss their effect on delay, noise, and signal integrity.	CO5	L2	5M

UNIT-IV

8	a	Explain in detail about parity generator.	CO4	L2	5M
	b	Design a Comparatór using a tree-based logic structure.	CO5	L3	5M

OR

9	a	Explain the Semi-Custom and Full-Custom methodologies.	CO5	L2	5M
	b	Explain CPLD architecture.	CO5	L3	5M

UNIT-V

10	a	Explain the trade-offs between area overhead, performance degradation, and fault coverage in DFT techniques.	CO6	L5	5M
	b	Describe Built-In Self-Repair (BISR) in memory testing.	CO6	L3	5M

OR

11	a	Explain the procedure to do manufacturing test in detail.	CO4	L3	5M
	b	Discuss various types of delay faults in CMOS circuits.	CO6	L4	5M

***** END *****